**Pipeline Numerical**

**Ques-1** 4- Instructions are executed in a 4-stage pipelining. Assume that each instruction required different stage delay (in terms of number of clock cycle) as mentioned in the table below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **IF** | **ID** | **EX** | **WB** |
| **I1** | 1 | 2 | 2 | 2 |
| **I2** | 2 | 3 | 3 | 1 |
| **I3** | 2 | 1 | 3 | 1 |
| **I4** | 1 | 4 | 2 | 2 |

**Sol:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 |
| IF | I1 | I2 | I2 | I3 | I3 | I4 |  |  |  |  |  |  |  |  |  |  |
| ID |  | I1 | I1 | I2 | I2 | I2 | I3 | I4 | I4 | I4 | I4 |  |  |  |  |  |
| EX |  |  |  | I1 | I1 | - | I2 | I2 | I2 | I3 | I3 | I3 | I4 | I4 |  |  |
| WB |  |  |  |  |  | I1 | I1 | - | - | I2 | - | - | I3 | - | I4 | I4 |

**16 cyles**

**Nonpipelined=7+9+7+9= 32cycle**

**Speedup= 32/16 ~2**

**Ques-2** A 4-Stage pipeline has the stage delay of 150ns, 120ns, 160ns and 140ns respectively. Register that are used b/w the stages have a delay of 5ns each. Assuming constant clocking rate, what is the total time taken by pipeline to process 1000 data items.

Tp= max(150,120,160,140) + 5ns

= 160 +5 ns= 165ns

Total time= tp(n+k-1)

= 165(1000+ 4-1)

=165 (1000 +3)

= 165.5 micro sec

**Ques-3** 5-functional units operate using pipelining with clock cycle delay 10ns, 8ns, 10ns, 10ns, 7ns. Assume pipelines have a 1ns overhead. Find the speedup factor.

Tp=10+1=11ns

Non pipelined tpn= 10+8+10+10+7+1=45ns

Speedup = 45/11~4times

**Instruction Pipeline**

4- Instructions are executed in a 4-stage pipelining. Assume that each instruction required different stage delay (in terms of number of clock cycle) as mentioned in the table below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **IF** | **ID** | **EX** | **WB** |  |
| **I1** | 1 | 3 | 2 | 1 | 7 |
| **I2** | 2 | 2 | 3 | 1 | 8 |
| **I3** | 1 | 1 | 1 | 1 | 4 |
| **I4** | 2 | 1 | 1 | 2 | 6 |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 |
| IF | I1 | I2 | I2 | - | I3 | I4 | I4 |  |  |  |  |  |  |
| ID |  | I1 | I1 | I1 | I2 | I2 | I3 | I4 |  |  |  |  |  |
| EX |  |  |  |  | I1 | I1 | I2 | I2 | I2 | I3 | I4 |  |  |
| WB |  |  |  |  |  |  | I1 | - | - | I2 | I3 | I4 | I4 |

Answer-13 clock cycle

Speed up= tnp/tp = 7+8+4+6/13 = 25/13 ~ 2